Amendments to the Specification:

Replace the title at page 2, lines 1 with the following:

PROCESSOR WITH COPROCESSOR TO EXECUTE UNSUPPORTED INSTRUCTIONS

Rewrite paragraph **[0001]** at pages 2 and 3 as follows:

This application claims priority to U.S. Provisional Application Serial No. 60/400,391 titled "JSM Protection," filed Jul. 31, 2002, incorporated herein by reference. This application also claims priority to EPO Application No. 03291924.3, filed Jul. 30, 2003 and entitled "Inter-Processor Control," incorporated herein by reference. This application also may contain subject matter that may relate to the following commonly assigned co-pending applications incorporated herein by reference: "System And Method To Automatically Stack And Unstack Java Local Variables," ~~Ser. No. _____~~, filed Jul. 31, 2003, now U.S. Patent 7,069,415~~Attorney Docket No. TI-35422 (1962-05401)~~; "Memory Management Of Local Variables," Ser. No. 10/632,067, filed Jul. 31, 2003~~, Attorney Docket No. TI-35423 (1962-05402)~~; "Memory Management Of Local Variables Upon A Change Of Context," Ser. No. 10/632,076, filed Jul. 31, 2003~~, Attorney Docket No. TI-35424 (1962-05403)~~; "A Processor With A Split Stack," ~~Ser. No. _____~~, filed Jul. 31, 2003, now U.S. Patent 7,058,765~~Attorney Docket No. TI-35425(1962-05404)~~; "Using IMPDEP2 For System Commands Related To Java Accelerator Hardware," Ser. No. 10/632,069, filed Jul. 31, 2003~~, Attorney Docket No. TI-35426 (1962-05405)~~; "Test With Immediate And Skip Processor Instruction," Ser. No. 10/632,214, filed Jul. 31, 2003~~, Attorney Docket No. TI-35427 (1962-05406)~~; "Test And Skip Processor Instruction Having At Least One Register Operand," Ser. No. 10/632,084, filed Jul. 31, 2003~~, Attorney Docket No. TI-35248 (1962-05407)~~; "Synchronizing Stack Storage," Ser. No. 10/631,422, filed Jul. 31, 2003~~, Attorney Docket No. TI-35429 (1962-05408)~~; "Methods And Apparatuses For Managing Memory," Ser. No. 10/631,252, filed Jul. 31, 2003~~, Attorney Docket No. TI-35430 (1962-05409)~~; "Write Back Policy For Memory," Ser. No. 10/631,185, filed Jul. 31, 2003~~, Attorney Docket No. TI-35431 (1962-05410)~~; "Methods And Apparatuses For Managing Memory," Ser. No. 10/631,205, filed Jul. 31, 2003~~, Attorney Docket No. TI-35432 (1962-05411)~~; "Mixed Stack-Based RISC Processor," Ser. No. 10/631,308, filed Jul. 31, 2003~~, Attorney Docket No. TI-35433 (1962-~~

~~05412~~); "Processor That Accommodates Multiple Instruction Sets And Multiple Decode Modes," Ser. No. 10/631,246, filed Jul. 31, 2003~~, Attorney Docket No. TI-35434 (1962-05413)~~; "System To Dispatch Several Instructions On Available Hardware Resources," Ser. No. 10/631,585, filed Jul. 31, 2003~~, Attorney Docket No. TI-35444 (1962-05414)~~; "Micro-Sequence Execution In A Processor," Ser. No. 10/632,216, filed Jul. 31, 2003~~, Attorney Docket No. TI-35445 (1962-05415)~~; "Program Counter Adjustment Based On The Detection Of An Instruction Prefix," Ser. No. 10/632,222, filed Jul. 31, 2003~~, Attorney Docket No. TI-35452 (1962-05416)~~; "Reformat Logic To Translate Between A Virtual Address And A Compressed Physical Address," Ser. No. 10/632,215, filed Jul. 31, 2003~~, Attorney Docket No. TI-35460 (1962-05417)~~; "Synchronization Of Processor States," Ser. No. 10/632,024, filed Jul. 31, 2003~~, Attorney Docket No. TI-35461 (1962-05418)~~; "Conditional Garbage Based On Monitoring To Improve Real Time Performance," Ser. No. 10/631,195, filed Jul. 31, 2003~~, Attorney Docket No. TI-35485 (1962-05419)~~; "Cache Coherency In A Multi-Processor System," ~~Ser. No. _____~~, filed Jul. 31, 2003, now U.S. Patent 6,996,683~~Attorney Docket No. TI-35637 (1962-05421)~~; "Concurrent Task Execution In A Multi-Processor, Single Operating System Environment," Ser. No. 10/632,077, filed Jul. 31, 2003~~, Attorney Docket No. TI-35638 (1962-05422)~~; and "A Multi-Processor Computing System Having A Java Stack Machine And A RISC-Based Processor," Ser. No. 10/631,939, filed Jul. 31, 2003~~, Attorney Docket No. TI-35710 (1962-05423)~~.

Rewrite paragraph **[0023]** at page 11 as follows:

In the step-by-step mode, the second processor fetches a supported instruction from memory 206 through memory bus 222, and loads the instruction in the decode logic 210 of the first processor 202. In at least some embodiments, the switch 230 closes when the first processor 202 transitions to the step-by-step mode so that the control logic ~~210~~ 218 is connected to port 214 and may be accessed by the second processor 204. The switch 230 may comprise any electrical apparatus for controlling the coupling of port 214 to decode logic 210. The second processor 204 may load supported instructions to the decode logic 210 of the first processor 202 using a memory mapped instruction buffer, co-processor instruction, or other instruction, wherein the supported instructions are sent from the second processor 204 via the inter-processor

bus 220, port 214, and switch 230 to the decode logic 210 of first processor 204 for decoding and subsequent execution in the first processor 202.